## REMARKS

Applicants respectfully traverse and request reconsideration.

Claim 21 stands rejected under 35 U.S.C. § 112, second paragraph as being indefinite due to a typographical error. Applicants have corrected the typographical error in claim 21.

Claims 1, 2, 4, 6, 8-10, 13-15 and 18 stand rejected under 35 U.S.C § 103(a) as being unpatentable over Applicant's admitted prior art, in view of U.S. Patent No. 6,067,272 (Foss).

In the "Response to Arguments" section, the Office Action states that it would be obvious for one of ordinary skill in the art to replace the clock signal period dividing circuit 22 of admitted prior art, with the teachings of Foss because doing so would allow the system in the prior art to compensate for delay variations. Applicants respectfully submit that the Foss reference must be considered for what it actually teaches. The delay in Foss is used to compensate for delays for the input clock signal. Foss does not contemplate, teach or suggest the additional compensation or even a need to compensate for delays associated with a receive path of a STROBE signal wherein the receive path already includes an additional variable delay circuit. To the contrary, Foss specifically teaches to use a delay model activation an enable buffer to output information from memory. The delay model uses "similar elements as the real circuit path taken by the input clock signal." Stated another way, the Foss reference does not contemplate compensating a clock input and a STROBE input nor compensating for delay variations associated with a phase shifted output signal drive buffer located in a variable delay circuit that receives a STROBE signal as claimed. Accordingly, the independent claims are believed to be allowable for at least these reasons.

In addition, the dependent claims add additional novel and nonobvious subject matter and are also believed to be in condition for allowance since they add additional novel and non obvious subject matter.

For example, as to claim 21, it appears that claim language is being overlooked. The Office Action states that simply because Foss teaches a DLL that can include Serially coupled buffered stages, that such as structure may obviate Applicant's invention. However, as noted, Foss is not directed to putting a clock input in the STROBE input nor compensating for delay variations associated with the phase shifted output signal driver buffer located in a variable delay circuit that receives a strobe signal. The claim requires a delay lock loop group circuit responsive to a reference signal and the feedback control signal and wherein the feedback delay matching delay includes buffer stages that compensate for delay variations associated with both the phase shifted output signal drive buffer and multiplexing circuit in a STROBE signal receive path. Applicant's admitted prior art fails to show such structure and Foss fails to show such structure and the combination thereof also fails to show or suggest this structure. Accordingly, Applicants respectfully submit that this claim is also in condition for allowance.

Applicants respectfully submit that the claims are in condition for allowance and respectfully request that a timely Notice of Allowance be issued in this case. The Examiner is invited to contact the below listed attorney if the Examiner believes that a telephone conference will advance the prosecution of this application.

Respectfully submitted,

Date: 12-9-04

By: _____
Christopher J. Reckamp
Registration No. 34,414

Vedder, Price, Kaufman & Kammholz, P.C.
222 N. LaSalle Street
Chicago, Illinois 60601
PHONE: (312) 609-7599
FAX: (312) 609-5005